

Microelectronics Systems Design ECE 446
Fall 2003 Test 2

1. Name and draw the standard symbol for the 8 standard logic gates. (8 points)

2. Define the logical operation performed by an AOI-32 gate (4 points)

3. Draw the transistor schematic and standard symbol of a CMOS transmission gate. (3 points)

4. Identify the three states of a tri-state buffer. (3 points)

5. Describe the three modes of power consumption for CMOS systems. (6 points)

6. What are the two mechanisms (dynamic and static) for information storage (memory) in a CMOS circuit? (4 points)

7. Describe the differences between a *latch* and a *flip-flop*. (4 points)

8. Define (3 points each)

(a) non-overlapping clock

(b) glitch

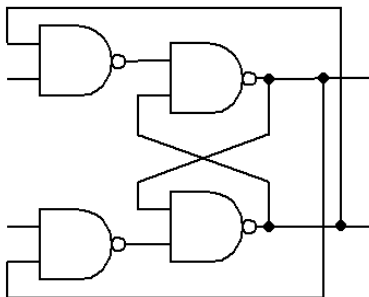
(c) euler path

(d) fan-out

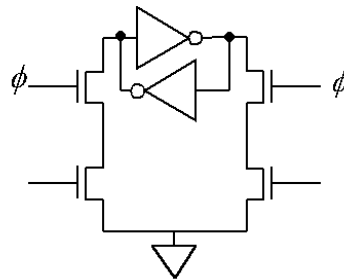
9. CMOS pull-down networks are designed in _____ transistors and pull-up networks in _____ transistors. These two networks are _____ (2 points)

10. Design a D-latch from two inverters and two transmission gates. Identify your design as dynamic or static. (5 points)

11. Identify the following components. (4 points)



(a) _____



(b) _____

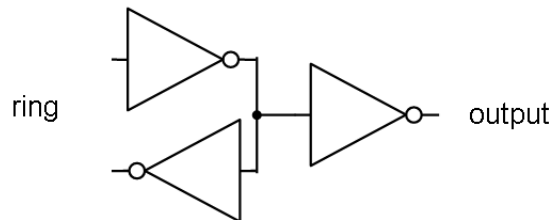
Microelectronics Systems Design ECE 446

Fall 2003 Test 2

12. Given the following data for an inverter driving a load capacitance.

C_{load} (fF)	delay (ps)
20	200.1
40	331.5
80	594.3

- Find (a) the output capacitance of the inverter, (b) the effective resistance of the inverter, and (c) the input capacitance of the inverter if using a second identical inverter as a load gives a delay of 255 psec for the first inverter. (10 points)
13. Calculate the frequency of a 21-inverter ring oscillator if the delay of one inverter is 255 psec. (5 points)
14. A simple ring oscillator above has no way to couple the signal to an output port. Suppose one additional inverter is connected as shown. Given the information from previous problems, calculate the change in the frequency of the oscillator. (5 points)



15. Draw and label the circuit diagram of a C²MOS (clocked CMOS) register and explain why it is relatively insensitive to clock overlap. (5 points)
16. Draw and label the circuit diagram of a Schmidt trigger. Briefly explain how it operates (10 points)
17. Design a CMOS circuit to generate the logic function $\overline{((A + B)C)}$. Draw a transistor circuit diagram for your design. Graduate students should create a SPICE simulation for this circuit. Submit a powerpoint or word document showing the schematics and probe results for your simulation. Use hierarchical schematics in your layout. (10 points)