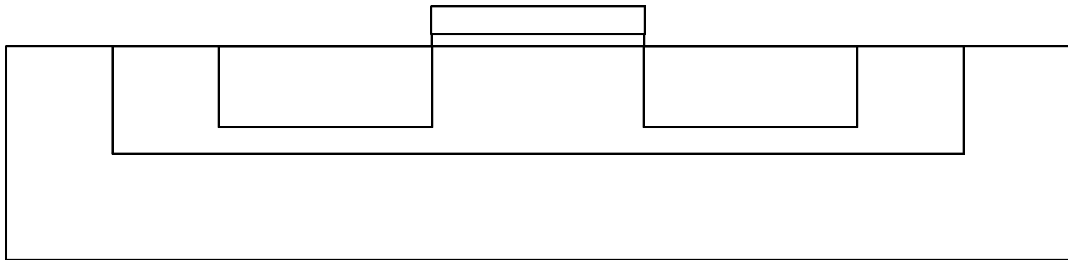


**Microelectronics Systems Design ECE 446**  
**Fall 2003 Test 1**

1. What is the value of  $\lambda$  for a  $0.18\mu\text{m}$  process? (5 points)
2. Decode the following acronyms associated with microelectronics (1 point each)
  - (a) ASIC
  - (b) CMOS
  - (c) DRC
  - (d) MOSFET
  - (e) VLSI
3. The diagram below is supposed to be the cross-section of an PMOS transistor in a well. Label the gate, substrate, gate oxide, diffusion areas, well, source, and drain. Mark  $n^+$  or  $p^+$  as appropriate. (5 points)



4. In the PMOS transistor above, should you connect the well to  $V_{dd}$  (+ supply voltage) or  $V_{ss}$  (ground)? (3 points)
5. In making the well connection above, should you use contacts to  $p^+$  or  $n^+$  active regions? (2 points)
6. Explain the difference between field oxide and gate oxide. (2 points)
7. How do you connect metal2 to poly layers? (3 points)

8. Define (3 points each)

(a) planarization

(b) channel-stop implant (or field implant)

(c) velocity saturation

(d) ion implantation

(e) etching

9. Suppose a foundry suggested a limit of  $0.5 \text{ ma}/\mu\text{m}$  for metal wires due to metal migration? Why might this limit be imposed? How would it affect your design of a wire intended to carry 3 mA? (3 points)

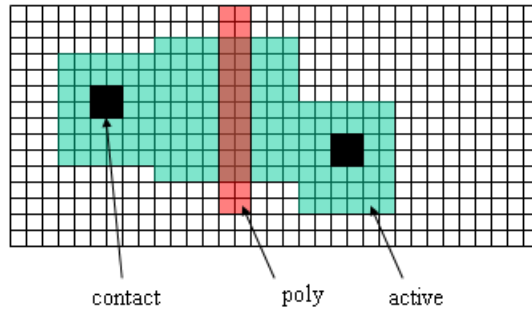
10. Explain the usage of active regions and select regions in the layout of a transistor using MOSIS scalable design rules. (2 points)

11. Draw the circuit diagram of an inverter. Label the input, output nodes and the connections to power and ground rails Show the body connections explicitly. (5 points)

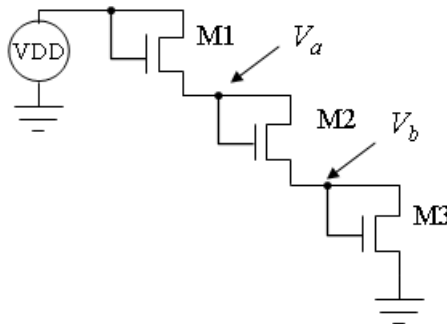
12. Draw the circuit diagram for two NMOS transistors in parallel. Do you add the widths or the lengths (or both) to obtain the equivalent single transistor? (5 points)

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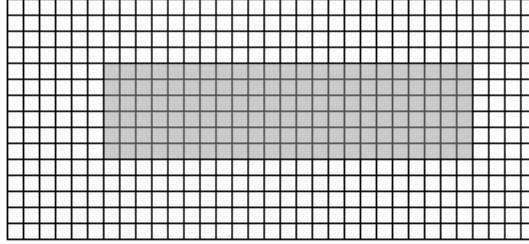
13. The diagram below shows a transistor (poly over  $n^+$ ) with a grid spacing of one  $\lambda$  square. Assume a process with  $\lambda = 0.8 \mu\text{m}$ .



- (a) Find  $W$  and  $L$  for the transistor. (5 points)
- (b) Find the area  $AD$  and perimeter  $PD$  for the drain. Assume the drain is the active area on the right. (5 points)
14. Analyze the circuit below in Spice. Make the transistors  $W=4.8\mu\text{m}$  and  $L=1.6\mu\text{m}$ . Use the AMI-ABN process and use proper body connections.  $V_{DD} = 5 \text{ v}$ . Show your final layout. Find voltages  $V_a$  and  $V_b$  and the current flowing through the transistors. (15 points)



15. Assume the wire below is formed with a process for which  $\lambda = 0.25\mu\text{m}$ . The grid-line spacing is one  $\lambda$ .



- (a) Given  $R = 20\Omega/\square$ , find the wire resistance. (5 points)
- (b) Given plate  $C_{bw} = 70 \text{ aF}/\mu\text{m}^2$  and fringe  $C_{sw} = 30 \text{ aF}/\mu\text{m}$ , find the total capacitance. (5 points)
16. Given the parameters in the table below

VTO	zero-bias threshold voltage	$V_{T0}$	0.8 V
GAMMA	body-effect parameter	$\gamma$	0.6
PHI	surface to bulk potential	$2 \phi_F $	0.6 V
CJ0	bottom wall depletion capacitance	$C_{j0}$	$4 \cdot 10^{-4} \text{ F/m}^2$
MJ	bottom wall grading coefficient	$m$	0.43
PB	bottom built-in potential	$\phi_0$	0.74 V

- (a) Find the threshold voltage if  $V_{sb} = 3\text{V}$  (5 points)
- (b) Convert CJ0 to units of  $\text{fF}/\mu\text{m}^2$ . (2 points)
- (c) Find the bottom capacitance of the source if  $V_{sb} = 3\text{V}$  and  $\text{AS} = 50\text{p}$ . Note that the equivalent diode is reversed biased ( $V_D$  is negative). (3 points)