

Microelectronics Systems Design ECE 446
Fall 2001 Test 3

1. Draw a diagram illustrating the design of a precharge-evaluate logic gate and explain the principles of operation. (10 points)

2. Identify the following acronyms (1 point each)
 - (a) ALU
 - (b) JTAG
 - (c) CAM
 - (d) ESD
 - (e) FPGA

3. Draw the circuit diagram of a static memory element showing the word line, bit and $\overline{\text{bit}}$ lines, and inverter elements. (10 points)

4. Define (3 points each)

(a) standard cell

(b) tri-state buffer

(c) two-bit function block

(d) tree decoder

(e) shift register

5. Explain the terms controllability and observability in the context of testing. (5 points).

6. Explain the design concepts of regularity, modularity, and locality. (5 points)

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7. Explain why ESD is a problem, and summarize the three basic models for ESD testing. (10 points)

8. Explain the differences between the use of resistors and active pull-ups (e.g. pseudo-NMOS) in designing ratioed logic. (10 points)

9. Explain how the p-sense and n-sense amplifiers are used to read from a dynamic memory cell. (10 points)

10. Summarize the five common IC package types. (5 points)

11. Explain PTH and SMT packaging. (5 points)

12. Define the concept of *clock skew* and describe two techniques for minimizing clock skew. (10 points)