

Microelectronics Systems Design ECE 446
Fall 2001 Test 2

1. What are the design principles for pullup/pulldown complementary networks? (5 points)

2. Define the logical operation performed by an AOI-32 gate (5 points)

3. Draw the transistor schematic and standard symbol of a CMOS transmission gate? (4 points)

4. Explain the difference between a latch and a flip-flop (4 points)

5. What are the two mechanisms (dynamic and static) for information storage (memory) in a CMOS circuit? (4 points)

6. Draw the transistor schematic of a clocked inverter. Label the input, output, and clock signals. (4 points)

7. Name and draw the standard symbol for the 8 standard logic gates. (8 points)

8. Define (3 points each)

(a) SR latch

(b) glitch

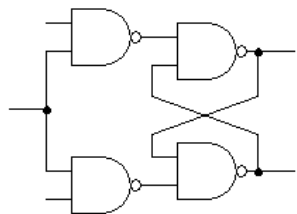
(c) shift register

(d) master-slave flip-flop

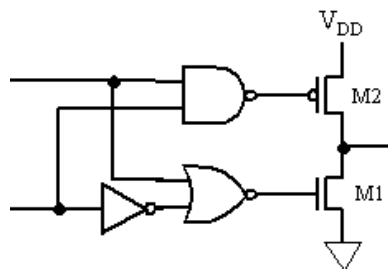
9. Design a 4-1 multiplexer using transmission gates. Show your results as a logic diagram using the standard logic symbol for a transmission gate. Label the control signals as S_1 and S_0 , the inputs as $A \cdots D$, and the output as OUT. (5 points)

10. Design a D-latch from an SR-latch and an inverter. (5 points)

11. Identify the following components. (4 points)



(a) _____



(b) _____

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12. Design a CMOS circuit for an XOR gate, using transmission gates and inverters. Show the resulting transistor circuit. (10 points)

13. Calculate the frequency of a 51-inverter ring oscillator if the delay of one inverter is 300 psec. (5 points)

14. Describe the three modes of power consumption for CMOS systems. (10 points)

15. Suppose 4 stages are used to drive a 20 pF external load assuming that $C_g = 30\text{fF}$ for the smallest inverter. How big are the transistors in the last inverter relative to the first inverter? (5 points)

16. Consider a uniform polysilicon wire with a length of $500\ \mu\text{m}$ and a width of $2\ \mu\text{m}$. Assume a sheet resistance of $25\ \Omega/\text{square}$ and a plate capacitance of $0.08\ \text{fF}/(\mu\text{m})^2$. Find the Elmore propagation delay from one end of the wire to the other. (5 points)

17. Design a CMOS circuit to generate the logic function $\overline{((A+B)C)+D}$. Draw a transistor circuit diagram for your design. (5 points)