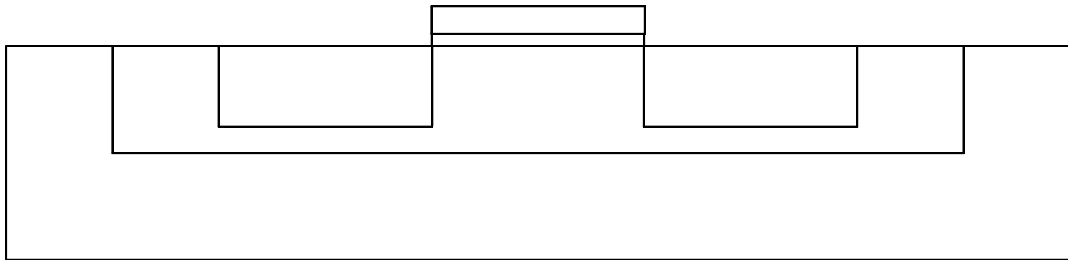


Microelectronics Systems Design ECE 446
Fall 2001 Test 1

1. What is the value of λ for a $1.2\mu\text{m}$ process? (5 points)
2. Decode the following acronyms associated with microelectronics (1 point each)
 - (a) ASIC
 - (b) CMOS
 - (c) DRC
 - (d) MOSFET
 - (e) VLSI
3. The diagram below is supposed to be the cross-section of an PMOS transistor. Label the gate, substrate, gate oxide, diffusion areas, well, source, and drain. Mark n^+ or p^+ as appropriate. (5 points)



4. In the PMOS transistor above, should you connect the well to Vdd (+ supply voltage) or Vss (ground)? (3 points)
5. In making the well connection above, should you use contacts to p^+ or n^+ active regions? (2 points)
6. Explain the difference between a contact and a via. (2 points)
7. How do you connect metal2 to poly layers? (3 points)

8. Define (3 points each)

(a) photoresist

(b) noise margin

(c) Moore's Law

(d) lithography

(e) poly

9. What is metal migration? What rule is imposed to prevent metal migration? (3 points)

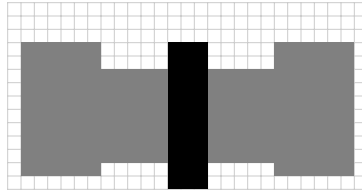
10. Explain the usage of active regions and select regions in the layout of a transistor using MOSIS scalable design rules. (2 points)

11. Draw the circuit diagram of an inverter. Label the input, output nodes and the connections to power and ground rails Show the body connections explicitly. (5 points)

12. Draw the circuit diagram for two NMOS transistors in series. Do you add the widths or the lengths (or both) to obtain the equivalent single transistor? (5 points)

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13. The diagram below shows a transistor (poly over n^+) on a $1\mu\text{m}$ grid.



- (a) Find W and L for the transistor. (5 points)
(b) Find the area AD and perimeter PD for the drain. (5 points)
14. Given the following information from an NMOS characteristic curve ($V_{GS} = 5$ Volts):

V_{DS} (V)	I_D (μA)
2.1	237.85
4.5	326.76
5.0	328.76

You may find the following formula useful:

$$\lambda = \frac{I_2 - I_1}{V_2 I_1 - V_1 I_2}$$

- (a) Find the transconductance κ and channel modulation λ for the simple (level 1) model that match the measured values in the saturation region of the table above. $V_T = 0.8$ V. (5 points)
- (b) Find the effective resistance of the transistor. (5 points)
- (c) Calculate the current I_D at $V_{DS} = 3$ V for the level 1 model. (5 points)

15. Assume the wire below is formed with a $\lambda = 0.5\mu\text{m}$ process. The grid-line spacing is one λ .



- (a) Given $R = 15\Omega/\square$, find the wire resistance. (5 points)
- (b) Given plate $C_{bw} = 45 \text{ aF}/\mu\text{m}^2$ and fringe $C_{sw} = 60 \text{ aF}/\mu\text{m}$, find the total capacitance. (5 points)
16. Given the parameters in the table below

VTO	zero-bias threshold voltage	V_{T0}	0.8 V
GAMMA	body-effect parameter	γ	0.6
PHI	surface to bulk potential	$2 \phi_F $	0.6 V
CJ0	bottom wall depletion capacitance	C_{j0}	$3 \cdot 10^{-4} \text{ F/m}^2$
MJ	bottom wall grading coefficient	m	0.43
PB	bottom built-in potential	ϕ	0.74 V

- (a) Find the threshold voltage if $V_{sb} = 2.5\text{V}$ (5 points)
- (b) Find the bottom capacitance of the source if $V_{sb} = 2.5\text{V}$ and $AS = 40\text{p}$ (5 points)