Computer Architecture ECE314
Winter 2006 Test 1

1. The fundamental gates are NOT, AND, OR, XOR. Draw and label the corresponding logic symbols and Verilog operators? (8 points)

2. Identify the following terms or abbreviations (2 points each)

   (a) ASCII

   (b) BCD

   (c) MSB

3. Convert 72_{10} to octal, hexadecimal and binary. (6 points)

4. Convert the binary number 01010011 to an 8-bit 2's-complement negative number. (3 points)

5. What are the differences between a static latch and a dynamic latch? (2 points)

6. Explain the hierarchical nature of a computer system. (5 points)

7. Define or explain the following terms (3 points each)

   (a) tri-state buffer

   (b) gray code

   (c) master-slave flip-flop

   (d) T flip-flop

8. How can you tell whether a Verilog module represents a state machine? (4 points)

9. Write a dataflow Verilog module to calculate
   C = A AND B if S = 1 and C = A OR B if S = 0. (4 points)

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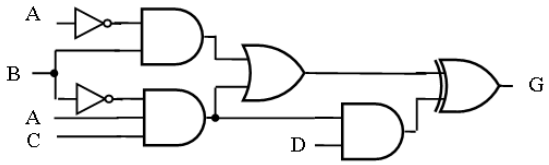
In each of the following problems, include comment lines at the start of each module with your name as author.

10. Write a structural Verilog module for the following logic operation. Use QUARTUS to compile and simulate your module. Submit a screen shot of the simulation, and a truth table for the logic operation. (25 points)



11. Write a Verilog model of the state machine shown below. Submit screen shot of a simulation, showing the input sequence 110010011. (25 points)