Computer Architecture ECE314
Winter 2006 Test 3

1. Write the expression $X + (Y * (W - Z))$ using Reverse Polish notation (stack oriented)? (4 points)

2. Explain the difference between a big-endian and a little-endian system. (3 points)

3. Name three different input devices (other than a mouse) used for rapid screen position location (pointing). (3 points)

4. Rank the following devices in order of data rate (bits/sec). (5 points)
   (a) Laser printer
   (b) Keyboard
   (c) Hard Disk
   (d) Video/graphics display
   (e) Modem
   (f) Mouse

5. Explain the terms latency and throughput as applied to a computer pipeline. (4 points)

6. Describe how interrupts are implemented as part of the fetch-execute cycle. (4 points)

7. Name two I/O techniques (other than interrupt-intiated I/O) (2 points)

8. Explain the principle of *locality* (spatial and temporal) with respect to cache memory. (4 points)

9. What is L1 and L2 cache?(4 points)

10. Given a hard disk with 512-byte sectors, 1024 sectors per track, 8000 tracks per surface, and 8 platter-surfaces, find the unformatted disk capacity. (4 points)

11. If the disk above rotates at 7200 rpm, find the rotational latency (in milliseconds) (2 points)

12. What is a *load-store* architecture? (2 points)

13. A computer has a 32-bit word length, and all instructions are one word in length. The register file of the computer has 16 registers. For a format with two register fields, one memory field, and a maximum of 50 opcodes, what is the maximum number of memory address bits available? (3 points)

14. A computer has a 32-bit instruction word broken into fields as follows: opcode 4-bits; two register fields, 6 bits each; and one immediate operand field, 16 bits. Assume that the opcode for this format must have the form 4'b1xxx. Find (2 point each)

    (a) the maximum number of operations that can be specified.

    (b) how many registers can be addressed

    (c) the range of signed immediate operands that can be provided.

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1. Explain the basic operation of an associative cache compared to a direct-mapping cache. (4 points)

2. Explain the following virtual memory concepts (3 points each)

   (a) overlays

   (b) partitions

   (c) paging

   (d) segmentation

3. Explain the terms thrashing and fragmentation as applied to a virtual memory system. (4 points)

4. A program consisting of a sequence of 15 instructions without branch or jump instructions is to be executed in a five-stage pipelined computer with a clock period of 1.4 ns. Determine the following (3 points each)

   (a) the latency time for the pipeline

   (b) maximum throughput for the pipeline

   (c) time required for executing the program

5. The program in a computer program compares two signed 2's complement numbers A and B by performing subtraction $A - B$ and updating the status bits. Let $A = 11011110$ and $B = 01110110$. Find the values of status bits N (sign), Z (zero), and V (overflow) (3 points)

6. A cache memory has an assess time from the CPU of 3 ns, and the main memory has an access time from the CPU of 30 ns. What is the effective access time for the cache main memory if the hit ratio is 0.85? (3 points)

7. Explain how handshaking works in a I/O process. (4 points)

8. How many characters per second can be transmitted over a 57,600-baud line for asynchronous serial transmission with one stop bit? Assume a character code of eight bits. (3 points)

9. Estimate the time required to read or write a block of 4 MB (2^{22} bytes) from disk to memory given the following disk parameters: seek time, 8.5 ms; rotational latency, 4.2 ms; controller time, negligible; transfer rate 160 MB/s (3 points)

10. ZigBee is a combination of HomeRF Lite and IEEE 802.15.4 protocols. It operates in the 2.4GHz (ISM) radio band - the same band as the IEEE 802.11b standard and Bluetooth. Zigbee is capable of connecting 255 devices per network. What is the data transmission rate of ZigBee? How does this compare to IEEE 802.11b and Bluetooth? What are the primary applications and advantages of ZigBee? (5 points)