Computer Architecture ECE314
Winter 2005 Test 1

1. The fundamental gates are NOT, AND, OR, XOR. Draw and label the corresponding logic symbols and Verilog operators? (8 points)

2. Identify the following terms or abbreviations (2 points each)

   (a) ASCII

   (b) BCD

   (c) MSB

3. Convert 38_{10} to octal, hexadecimal and binary. (6 points)

4. Convert the binary number 01001101 to an 8-bit 2's-complement negative number. (3 points)

5. What are the differences between a flip-flop and a latch? (2 points)

6. Explain the hierarchical nature of a computer system. (5 points)

7. Define or explain the following terms (3 points each)

   (a) tri-state buffer

   (b) gray code

   (c) master-slave flip-flop

   (d) finite state machine

8. How can you tell whether a Verilog module represents a state machine? (4 points)

9. Write a Verilog module to perform 2-1 multiplexor? (4 points)

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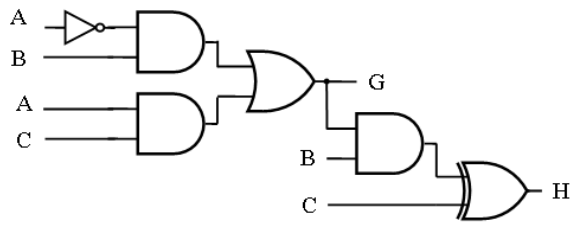
In each of the following problems, include comment lines at the start of each module with your name as author.

10. Write a structural Verilog module for the following logic operation. Use QUARTUS to compile your module and submit a one-page screen shot showing the Verilog source and compilation window. (20 points)



11. Write a behavioral Verilog module for a octal counter (0-7) using an **always** statement. Use QUARTUS to insure that your module compiles without errors. Submit a one-page screen shot showing the Verilog source and compilation window. (20 points)

12. Rewrite the following module to correct the syntax errors, and produce a successful compilation with QUARTUS. Submit a one-page screen shot as before. (10 points)

```
module 1st_exam(A,B,C,D,F)
inputs A, B, C;
Output D, F;
and g1(E,B,C);
not g2(d,E,A);
OR  g1(F,B,C);
endmodule;
```